

VITA 62 COMPLIANT VPX POWER SUPPLY



Outputs:

VS1:	}	+12V	/	80A	=	960W
VS2:						
VS3:		+5V	/	30A	=	150W
(AUX)		+3.3V _{AUX}	/	15A	=	50W
(AUX)		+12V _{AUX}	/	1A	=	12W
(AUX)		-12V _{AUX}	/	1A	=	12W

Features

- 90.0% typical efficiency (Vin=28V, full load)
- 18-36V continuous input voltage
- 1000W maximum total output power
- Input EMI filter
- Input reverse polarity protection
- -40°C to 85°C operating temperature (at card edge)
- Input over voltage, output over voltage, output over-current, short circuit, and over-temperature protections
- Current sharing on three main outputs
- Standard VITA 62 controls
- Optional I²C (IPMI/ PMBus/ VITA 46.11)
- Compliance:
 - VITA62
 - MIL-STD-704 (B-F)
 - MIL-STD-461
 - CE102 CS101 CS114
 - CS115 CS116
 - MIL-STD-810G
 - ESD Protection
 - Shock and Vibration
 - Rapid Decompression
 - Corrosion Resistance
 - Fungus Resistance
 - Altitude and Humidity

Part Numbering System

VPX	-	6U	-	1	D	1000	□	□
Series Name	-	Size (U)	-	Input Voltage Range		Output Power	Filter	I ² C Function
VPX	-	6U	-	1: 18-36V	D: DC input	1000: 1000W	P: EMI filter T: EMI filter with transient suppression	1: Without I ² C 2: With I ² C

Module Specific Specifications

Parameter	Notes & Conditions	Min.	Typ.	Max.	Unit
ABSOLUTE MAXIMUM RATINGS					
Input Voltage					
Non-Operating Input Voltage	Continuous	-50		60	V
Operating Input Voltage	Continuous			36	V
Operating Transient Protection	1s Transient, square wave			50	V
Isolation Voltage	Input to Output, Input to Case, Output to Case			1,500	V
Operating Temperature	Temperature at card edge	-40		85	°C
Storage Temperature		-55		105	°C
ELECTRICAL SPECIFICATIONS					
Input Voltage					
Continuous		18		36	V
Transient	50V Transient for 100ms	18		50	V
Input Under-Voltage Lockout					
Turn-On Threshold		16.5	17.0	17.5	V
Turn-Off Threshold		15.5	16.0	16.5	V
FEATURE SPECIFICATIONS					
VITA 62 ON/OFF Control					
Control signals referenced to SIGNAL_RETURN					
ENABLE* Logic High	ENABLE* is at high logic level if it's left open	2		3.6	V
ENABLE* Logic Low		0		0.8	V
INHIBIT* Logic High	INHIBIT* is at high logic level if it's left open	2		3.6	V
INHIBIT * Logic Low		0		0.8	V
RELIABILITY CALCULATIONS					
Calculated MTBF (MIL-217) MIL-HDBK-217F	Ground Benign (GB), 25°C ambient temperature		2,300		1000 hours
Calculated MTBF (MIL-217) MIL-HDBK-217F	Ground Mobile (GM), 25°C ambient temperature		130		1000 hours

Input Voltage Spikes

INPUT VOLTAGE SPIKE SUPPRESSION	
Module Operates Through these Spikes	
Input Voltage Spike (Centered on Vin)	
±250V, 100µs, Emax = 15mJ	MIL-STD-1275D
±200V, 10µs, Rs ≤ 0.5Ω	MIL-STD-461C (CS06); DEF-STAN 61-5
±400V, 5µs, Rs ≤ 0.5Ω	MIL-STD-461C (CS06)
±600V, 10µs, Rs = 50Ω	RTCA/DO-160E

Output Characteristics

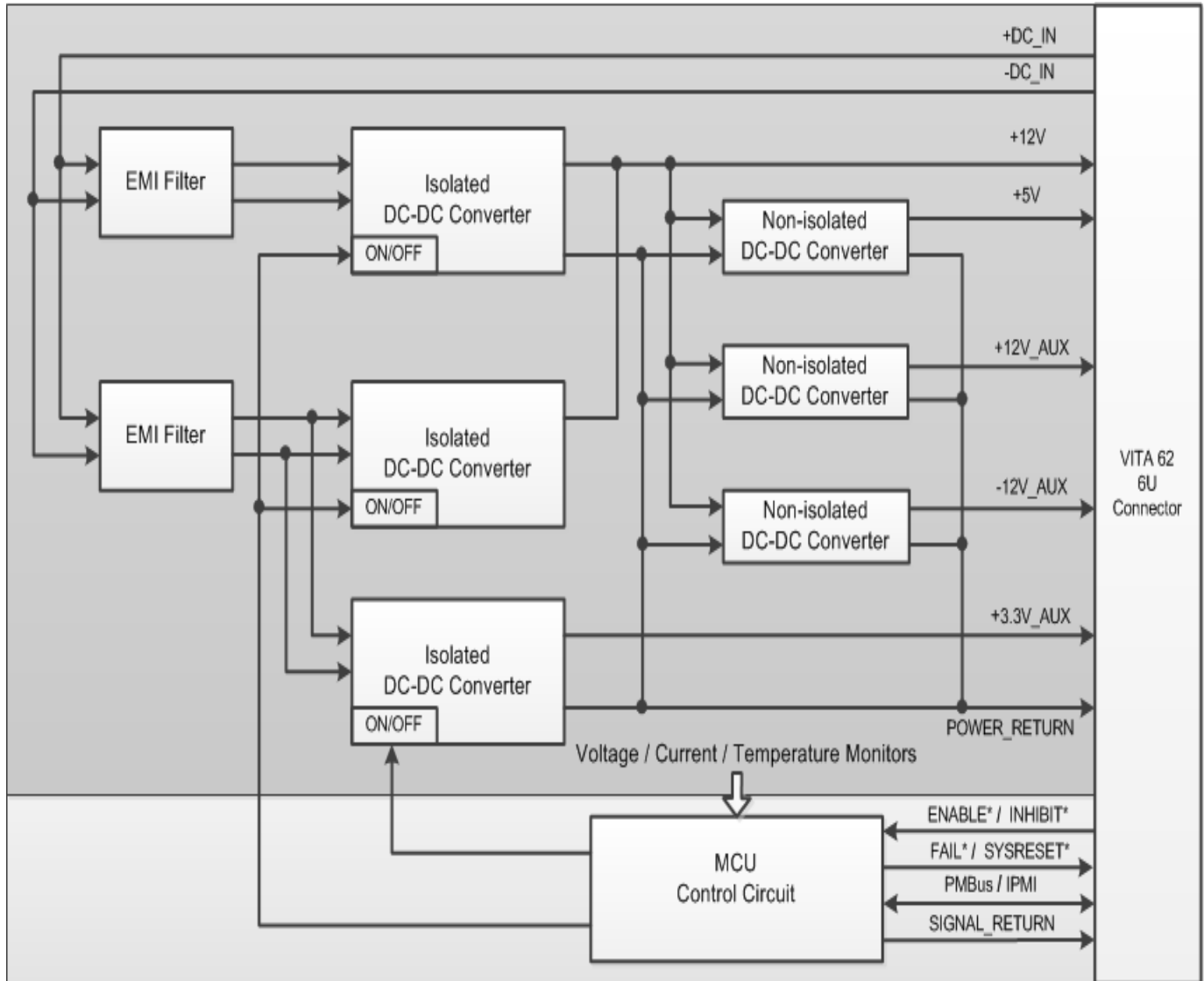
Parameter	+12V	+5V	+3.3V _{AUX}	+12V _{AUX}	-12V _{AUX}
OUTPUT CHARACTERISTICS					
Output Voltage Set Point 28Vin, 50% load	12V (±1%)	5V (±1%)	3.3V (±1%)	12V (±1%)	-12V (±1%)
Output Voltage Range Over line, load, temperature	12V (±3%)	5V (±3%)	3.3V (±3%)	12V (±3%)	-12V (±3%)
Output Voltage Ripple (peak-peak) Full load, measured with 1µF capacitor and 10µF tantalum capacitor.(5 Hz to 20 MHz bandwidth)	100mV	50mV	80mV	80mV	100mV
Output Current Range Total Output Power Limits to 1000W	0-80A	0-30A	0-15A	0-1A	0-1A
Output Over-Voltage Protection Set Point	14.8V	6V	4.5V	14.8V	N/A
Output Current-Limit Set Point	100A	45A	19A	2A	N/A
Maximum External Output Capacitance	4000uF	1000uF	2000uF	200uF	200uF
MAXIMUM TOTAL OUTPUT POWER	1000W				

Qualification Tests

TEST	STANDARD
Random Vibration	MIL-STD-810, 514.6 – Procedure I, Class V3
Shock	MIL-STD-810, 516.6 - Procedure I, VI, Class OS2
Altitude	MIL-STD-810, 500.5 - Procedure I, II, III
Fungus Resistance	MIL-STD-810, 508.6
Corrosion Resistance	ASTM G85, Annex A4
Humidity	MIL-STD-810, 507.5 - Procedure II
High Temperature	MIL-STD-810, 501.5 - Procedure I, II
Low Temperature	MIL-STD-810, 502.5 - Procedure I, II
Temperature Cycling	MIL-STD-202, 107 - Class C4
ESD	EN61000-4-2, Level 4; 15kV Air Discharge



Block Diagram





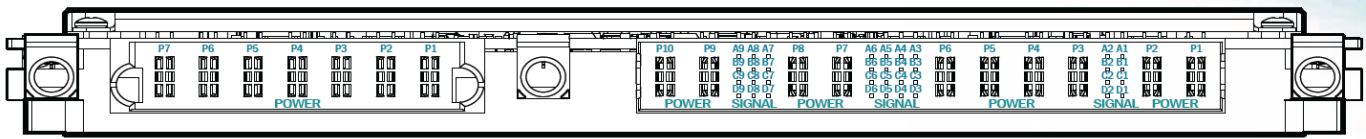
Features

Control States			
Control Inputs		State of Outputs	
ENABLE*	INHIBIT*	+3.3V_AUX	VS1,VS2,VS3 +12V_AUX, -12V_AUX
HIGH	HIGH	OFF	OFF
HIGH	LOW	OFF	OFF
LOW	HIGH	ON	ON
LOW	LOW	ON	OFF

At power-on, if ENABLE* and INHIBIT* are configured to turn all outputs on, +3.3V_AUX will be powered up 100ms prior to other outputs.

Parallel Operation	
+12V_MAIN & +5V_MAIN	+12V_MAIN and +5V_MAIN support active current sharing. For parallel operation of multiple converters, +12V_Share(+),+5V_Share(+), ENABLE* and INHIBIT* of all modules should be connected together respectively. It is suggested to have a ground plane on the system board for POWER_RETURN to reduce the ground noise impact on the current share accuracy. The loop formed by the trace connecting the Share pins and the ground trace should be minimized to avoid noise coupling into the current share circuitry. Adding capacitance to these share lines must be avoided.
+3.3V_AUX, +12V_AUX & -12V_AUX	These auxiliary outputs do not support active current sharing. However, all these auxiliary outputs have OR'ing MOSFETs or OR'ing diodes imbedded to support parallel operation. Total output current on any of the outputs should not exceed its current rating of a single module.

PIN Assignments



6U P0 Connector

PIN	FUNCTION	DESCRIPTION
P7	+DC_IN	Positive input voltage
P6	+DC_IN	Positive input voltage
P5	-DC_IN	Negative input voltage
P4	-DC_IN	Negative input voltage
P3	No Connection	
P2	No Connection	
P1	CHASSIS	Chassis

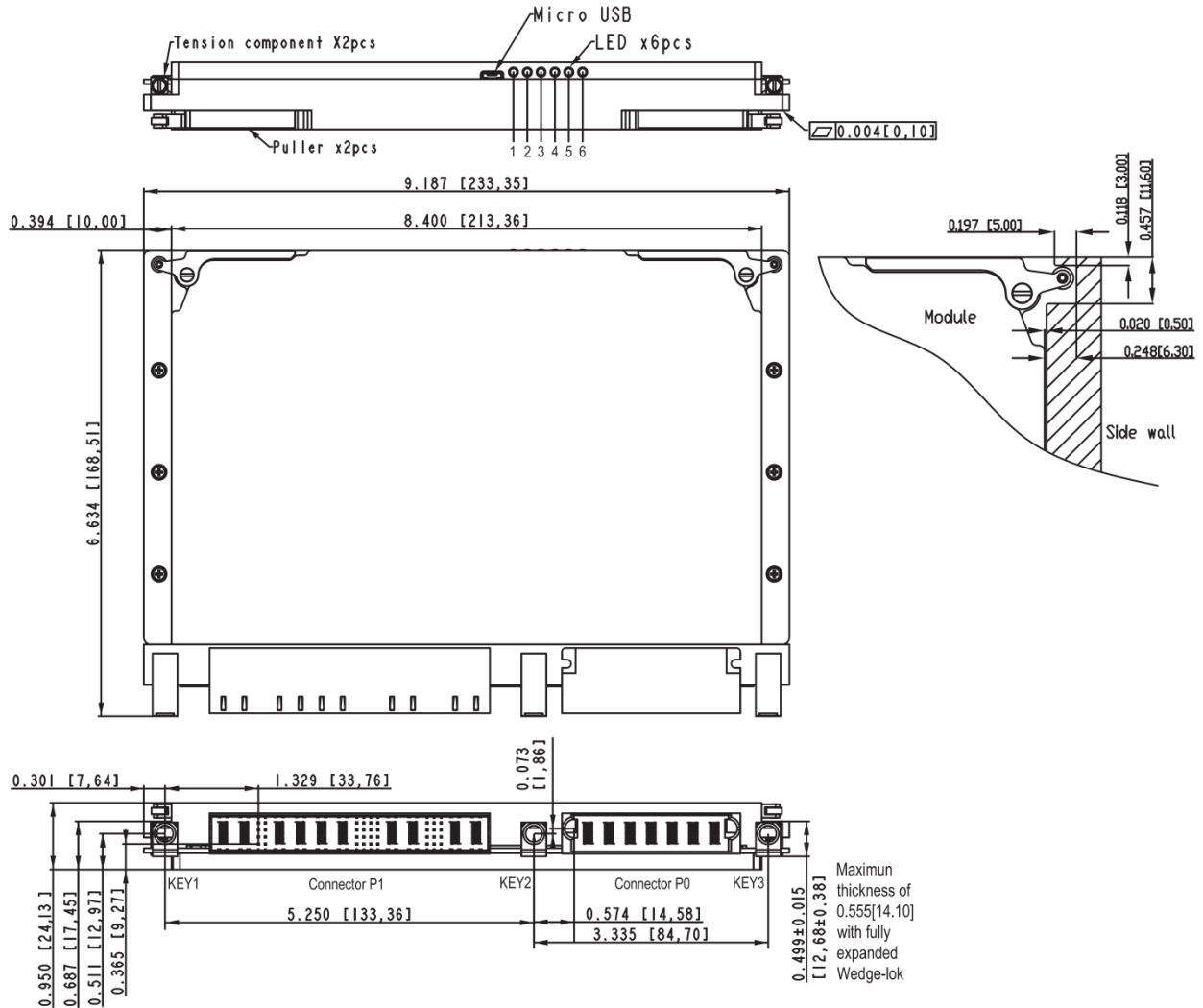
6U P1 Connector

PIN	FUNCTION	DESCRIPTION
P10	+12V_MAIN	+12V main output voltage, 80A rated
P9	+12V_MAIN	
A9	+12V_SENSE(+)	Should be connected to +12V_MAIN either remotely or at the connector
B9	+12V_SENSE(+)	
C9	+5V_SENSE(+)	Should be connected to +5V_MAIN either remotely or at the connector
D9	LED_DISABLE	Internally pulled up to 3.3V, connect to SIGNAL_RETURN to disable LED
A8	+12V_SENSE(-)	Should be connected to POWER_RETURN either remotely or at the connector
B8	+12V_SENSE(-)	
C8	No Connection	
D8	No Connection	
A7	+12V_SHARE(+)	Active current share differential pair for +12V_MAIN
B7	+12V_SHARE(-)	
C7	+5V_SHARE(+)	Active current share for +5V_MAIN
D7	SIGNAL_RETURN	Ground pin for control signals
P8	POWER_RETURN	Common output voltage return pin, 40A rated per pin
P7	POWER_RETURN	
A6	SM2	Redundant I ² C Clock Line, see Note1
B6	SM3	Redundant I ² C Data Line, see Note1
C6	-12V_AUX	-12V auxiliary output voltage, 1A rated
D6	SYSRESET*	System Reset is actively low. It will float when all outputs are within specification
A5	No Connection	
B5	No Connection	
C5	SM0	Primary I ² C Clock Line, see Note1
D5	SM1	Primary I ² C Data Line, see Note1
A4	No Connection	
B4	No Connection	
C4	GA1*	Geographical Address, see Note1
D4	GA0*	Geographical Address, see Note1
A3	No Connection	
B3	+12V_AUX	+12V auxiliary output voltage, 1A rated
C3	No Connection	
D3	No Connection	
P6	+5V_MAIN	+5V main output voltage, 30A rated
P5	+5V_MAIN	
P4	POWER_RETURN	Common output voltage return pin, 40A rated per pin
P3	POWER_RETURN	
A2	No Connection	
B2	FAIL*	When any of the output is not within specification, FAIL* signal will be driven low
C2	INHIBIT*	Input control signal as defined in VITA 62, referenced to SIGNAL_RETURN
D2	ENABLE*	Input control signal as defined in VITA 62, referenced to SIGNAL_RETURN
A1	No Connection	
B1	No Connection	
C1	I2C1_SMBA	Primary I2C Alert Line, see Note1
D1	I2C3_SMBA	Redundant I2C Alert Line, see Note1
P2	+3.3V_AUX	+3.3V auxiliary output voltage, 15A rated
P1	POWER_RETURN	Common output voltage return pin, 40A rated per pin

Note1: Refer to NetPower "VPX Communication Guide" for details.



Mechanical Drawing



Green LED Indication						Status	
1	2	3	4	5	6	ON	OFF
+12V	+5V	+3.3V AUX	+12V AUX	-12V AUX	MCU	Normal	Fault

Key Position	Alignment Angle	TE Connectivity Part Number
1	0°	1-1469492-1
2	0°	1-1469492-1
3	0°	1-1469492-1

Notes:

- 1) All dimensions in mm (inches)
- 2) Tolerances: $x \pm .5$ ($.xx \pm 0.02$)
 $.xx \pm .25$ ($.xxx \pm 0.010$)
- 3) Connector part numbers:
P0 – TE CONNECTIVITY 6450843-6
P1 – TE CONNECTIVITY 6450849-6
- 4) Weight: 3.8lbs (1.7kgs).
- 5) See table for key position for angle.
- 6) Flatness and surface finish requirement applies to both rails.